REMARKS

SUMMARY:

The present application sets forth claims 19-21 and 24-33, of which claims 19 and 25 are independent claims. Claims 34 and 35 are newly presented for consideration, and so the total active claims are 19-21 and 24-35.

Claims 19, 20, 21, 24 and 26 stand rejected under 35 U.S.C. §103(a) as being obvious over U.S. Patent No. 4,800,459 (Takagi et al.) in view of U.S. Patent Application Publication Nos. 2002/0145203 (Adae-Amoakoh et al.) and 2001/0038906 (O'Bryan et al.). Claims 25, 30 and 33 stand rejected under 35 U.S.C. §103(a) as being obvious over Takagi et al. in view of O'Bryan et al. Claims 27 and 28 stand rejected under 35 U.S.C. §103(a) as being obvious over Takagi et al. in view of Adae-Amoakoh et al. and O'Bryan et al. and further in view of U.S. Patent No. 5,512,710 (Schroeder). Claims 31 and 32 stand rejected under 35 U.S.C. §103(a) as being obvious over Takagi et al. in view of O'Bryan et al. and Schroeder.

Responses to the rejections summarized above (including traversal of the prior art rejections) are now presented with respect to each individual argument presented by the Examiner.

REJECTION OF CLAIMS 19, 20, 21, 24 and 26 (35 U.S.C. §103(a)):

Claims 19, 20, 21, 24 and 26 stand rejected under 35 U.S.C. §103(a) as being obvious over U.S. Patent No. 4,800,459 (Takagi et al.) in view of U.S. Patent Application Publication Nos. 2002/0145203 (Adae-Amoakoh et al.) and 2001/0038906 (O'Bryan et al.).

Claim 19 as presently amended sets forth a multi-layer electrical device including, in pertinent part, such elements as a first device layer, a second device layer with a plurality of via drilled therethrough, individual passive components vertically mounted into a selected of said plurality of via, and multiple portions of a non-conductive material respectively substantially filling the spaces defined by respective vias between each of the individual passive components and the second device layer. All such features, as affirmatively set forth in claim 19, particularly including the multiple

portions of non-conductive material as defined within the plurality of via, are not disclosed in the cited references nor rendered obvious thereby. Therefore, claim 19 cannot by law be unpatentable over such references.

As set forth in amended claim 19, the multiple portions of non-conductive material are provided in respective vias drilled through the second device layer. More particularly, the non-conductive material fills spaces defined by the vias around the individual passive components mounted into the vias and between such passive components and the second device layer. As such, there is a non-conductive wall including a passive component portion and the non-conductive filler material in each via of the multi-layer electrical device. As set forth in new dependent claim 34, one embodiment of such multiple portions of non-conductive material comprise insulative epoxy.

The provision of such portions of non-conductive material to partially encompass each passive component in the multi-layer electrical device of claim 19 effects several simultaneous advantages. A first such advantage corresponds to more securely positioning each individual passive component in place in its selected via location. A further advantage corresponds to preventing shorts between respective first and second opposing electrical terminations of each passive component. By sealing the passive components in place, the nonconductive material prevents any solder from running down the sides of the vias and shorting out the component or interfering with other electrical connections in the multilayer electronic device. Thus, unlike other conventional device vias, the device set forth in claim 19 provides vias that are not completely conducting throughout their length.

Takagi et al. does not disclose such additional non-conductive material for partially encompassing each passive component. In contrast, each layer 4-6 of Takagi et al. is formed with through-holes that are specifically designed such that the formation of respective chip-like components may be positioned and effectively formed therein. More particularly, for example, when it is desired to have two capacitors 26 and 27 and one resistor 28 as in the example illustrated in Figure 1, respective spaces 23-25 are

formed to specifically accommodate such preselected components. (Col. 1, lines 11-50).

The May 6, 2004 Office Action sets forth that Takagi et al. does disclose such multiple portions of non-conductive material (for example, in Figure 1). Furthermore, the August 15, 2003 Office Action sets forth on numbered page 6 with regard to Takagi et al. that "ceramic is utilized as the non-conductive material and it substantially fills the space between the passive components and the surrounding via. Additionally, it encases the passive component." Applicant respectfully disagrees with this assertion. The Examiner alleges that the ceramic laminated structure 10 in Takagi et al. corresponds to the first and second device layers set forth in present claim 19. The ceramic laminated structure 10 of Takagi et al. more particularly includes a plurality of ceramic layers 2-7 including ceramic layers 3-6 having cavities 44-49. The Examiner then proceeds with an assertion that the same ceramic material comprising the second device layers is the same as the non-conductive material set forth in claim 19 that substantially fills the space defined by the via between the individual passive components and the second device layer. Clearly, the second device layer and the non-conductive material set forth in claim 19 are different elements, and these different elements are not set forth in Takagi et al.

In contrast, only ceramic layers with cavities formed therein are disclosed in Takagi et al. Even if Takagi et al. were modified to provide additional material into the disclosed cavities, based on the disclosure of Takagi et al. such material would have to be a ceramic slurry material. Such ceramic slurry would then have to be sintered at temperatures that would effectively destroy surface resistor films when the passive components are resistors. For passive components such as capacitors and others, such high sintering temperatures would pose a severe risk of destroying or altering in an undesirable fashion the basic capacitance or other functional values of the passive components.

The multi-layer electrical device set forth in claim 19 as presently amended provides advantages to the technology disclosed in Takagi et al. The non-conductive filler material of claim 19 simultaneously secures the respective passive devices and

also prevents undesirable electrical shorting. No such provision is disclosed in Takagi et al. Furthermore, by providing vias that are not necessarily designed for respective specific components, a great amount of design versatility is afforded. As such, a plurality of different types and sizes of passive components can be positioned into each via and afterwards at least partially surrounded by non-conductive filler material. This eliminates the time-consuming and often costly need to form each via to suit particular device dimensions.

The above deficiencies of Takagi et al. as a reference are not overcome by the additional disclosure of Adae-Amoakoh et al. The high density chip carrier technology of Adae-Amoakoh et al. includes vertical connections (called vias or plated through holes (PTH)) 207 within a substrate core 22. These vias are commensurate with internal electrical connections that are completely conducting, similar to internal wires. Such conventional vias do not include features for significantly altering the electrical signal through the via, as is effected by the inclusion of passive components in the vias of claim 19. Furthermore, since the purpose of the vias in Adae-Amoakoh et al. is to be completely conducting, having a non-conductive wall in such via as set forth in claim 19 would destroy the signal carrying functionality of such vias 207. In regard to the basic requirements of a *prima facie* case of obviousness, §2143.01 of the MPEP sets forth that "if proposed modification would render prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification."

The above deficiencies of Takagi et al. and of Adae-Amoakoh et al. as references are also not overcome by O'Bryan et al. The circuit articles disclosed in O'Bryan et al., for example the flexible circuit described with respect to FIG. 4, includes holes 46 and 46' that are electroplated with copper to form surface copper structures 47 and 47'. Such electroplated structures effect solid conducting via connections, similar to the solid conducting vias of Adae-Amoakoh et al. These conductive structures disclosed in O'Bryan et al. also do not include features for significantly altering the electrical signal through the via, as is effected by the inclusion of passive components in the vias of present claim 19. Furthermore, since the purpose of the electroplated

structures in O'Bryan et al. is to be completely conducting, having a non-conductive wall in such via as set forth in present claim 19 would destroy the signal carrying functionality of such structures.

Claim 19 as presently amended also sets forth that the first and second device layers comprise an epoxy-fiberglass composite material. The May 6, 2004 Office Action correctly notes the lack of disclosure in Takagi et al. of such a material, and suggests that the technology of Takagi et al. could be modified to include the use of an epoxy-fiberglass composite material such as disclosed in O'Bryan et al. Applicant submits that modification of the circuit substrate of Takagi et al. to be made of an epoxy-fiberglass material (e.g., FR4) as disclosed in O'Bryan et al. would render the Takagi et al. reference unsatisfactory for its intended purpose. More particularly, utilization of an epoxy-fiberglass material such as FR4 in place of the disclosed green ceramic layers would destroy the functionality of the disclosed system. The epoxy-fiberglass composite material would not survive the high processing temperatures (on the order of about 900-1000 degrees Celsius) of the system disclosed in Takagi et al. (see col. 7, lines 1-3). Also, many passive components available at the time of the present invention and integrated with the electrical device set forth in claim 19 could not survive such high processing temperatures. In regard to the basic requirements of a *prima facie* case of obviousness, §2143.01 of the Manual of Patent Examining Procedure (MPEP) sets forth that "if proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification."

Since all of the elements set forth in claim 19 as presently amended are not disclosed singularly or in combination of the Takagi et al., Adae-Amoakoh et al. and O'Bryan et al. references, Applicant respectfully submits that present claim 19 is in condition for allowance and acknowledgement of the same is earnestly solicited. Also, Applicant respectfully traverses the 35 U.S.C. §103(a) rejection of claim 19 because there is no suggestion or motivation to combine the O'Bryan et al. and Takagi et al. references. More particularly, the proposed modification of Takagi et al., to incorporate the features set forth in O'Bryan et al. would destroy the intended function of Takagi et

al. Furthermore, since claims 20, 21, 24 and 26 variously depend from otherwise allowable claim 19 and further limit same, claims 20, 21 24 and 26 should also be allowable.

REJECTION OF CLAIMS 25, 30 and 33 (35 U.S.C. §103(a)):

Claims 25, 30 and 33 stand rejected under 35 U.S.C. §103(a) as being obvious over U.S. Patent No. 4,800,459 (Takagi et al.) in view of U.S. Patent Application Publication No. 2001/0038906 (O'Bryan et al.).

Claim 25 as presently amended sets forth a multi-layer electronic device including, in pertinent part, such elements as a plurality of first device layers, a plurality of second device layers each having a plurality of via drilled therethrough, individual passive components vertically mounted into a selected of said plurality of via, and multiple portions of a non-conductive material respectively substantially filling the spaces defined by respective vias between each of the individual passive components and the second device layers. All such features, as affirmatively set forth in claim 25, particularly including the multiple portions of non-conductive material as defined within the plurality of via, are not disclosed in the cited references nor rendered obvious thereby. Therefore, claim 25 cannot by law be unpatentable over such references.

As set forth in claim 25 as presently amended, the multiple portions of non-conductive material are provided in respective vias drilled through the second device layers. More particularly, the non-conductive material fills spaces defined by the vias around the individual passive components mounted into the vias and between such passive components and the second device layers. As such, there is a non-conductive wall including a passive component portion and non-conductive filler material in each via of the multi-layer electronic device. As set forth in new dependent claim 35, one embodiment of such multiple portions of non-conductive material comprise insulative epoxy.

The provision of such portions of non-conductive material to partially encompass each passive component in the multi-layer electronic device of claim 25 effects several simultaneous advantages. A first such advantage corresponds to more securely

positioning each individual passive component in place in its selected via location. A further advantage corresponds to preventing shorts between respective first and second opposing electrical terminations of each passive component. By sealing the passive components in place, the nonconductive material prevents any solder from running down the sides of the vias and shorting out the component or interfering with other electrical connections in the multilayer electronic device. Thus, unlike other conventional device vias, the device set forth in claim 25 provides vias that are not completely conducting throughout their length.

Takagi et al. does not disclose such additional non-conductive material for partially encompassing each passive component. In contrast, each layer 4-6 of Takagi et al. is formed with through-holes that are specifically designed such that the formation of respective chip-like components may be positioned and effectively formed therein. More particularly, for example, when it is desired to have two capacitors 26 and 27 and one resistor 28 as in the example illustrated in Figure 1, respective spaces 23-25 are formed to specifically accommodate such preselected components. (Col. 1, lines 11-50).

The May 6, 2004 Office Action sets forth that Takagi et al. does disclose such multiple portions of non-conductive material (for example, in Figure 1). Furthermore, the August 15, 2003 Office Action sets forth on numbered page 6 with regard to Takagi et al. that "ceramic is utilized as the non-conductive material and it substantially fills the space between the passive components and the surrounding via. Additionally, it encases the passive component." Applicant respectfully disagrees with this assertion. The Examiner alleges that the ceramic laminated structure 10 in Takagi et al. corresponds to the first and second device layers set forth in present claim 25. The ceramic laminated structure 10 of Takagi et al. more particularly includes a plurality of ceramic layers 2-7 including ceramic layers 3-6 having cavities 44-49. The Examiner then proceeds with an assertion that the same ceramic material comprising the second device layers is the same as the non-conductive material set forth in claim 25 that substantially fills the space defined by the via between the individual passive components and the second device layers. Clearly, the second device layers and the

non-conductive material set forth in claim 25 are different elements, and these different elements are not set forth in Takagi et al.

In contrast, only ceramic layers with cavities formed therein are disclosed in Takagi et al. Even if Takagi et al. were modified to provide additional material into the disclosed cavities, based on the disclosure of Takagi et al. such material would have to be a ceramic slurry material. Such ceramic slurry would then have to be sintered at temperatures that would effectively destroy surface resistor films when the passive components are resistors. For passive components such as capacitors and others, such high sintering temperatures would pose a severe risk of destroying or altering in an undesirable fashion the basic capacitance or other functional values of the passive components.

The multi-layer electronic device set forth in claim 25 as presently amended provides advantages to the technology disclosed in Takagi et al. The non-conductive filler material of claim 25 simultaneously secures the respective passive devices and also prevents undesirable electrical shorting. No such provision is disclosed in Takagi et al. Furthermore, by providing vias that are not necessarily designed for respective specific components, a great amount of design versatility is afforded. As such, a plurality of different types and sizes of passive components can be positioned into each via and afterwards at least partially surrounded by non-conductive filler material. This eliminates the time-consuming and often costly need to form each via to suit particular device dimensions.

The above deficiencies of Takagi et al. as a reference are not overcome by O'Bryan et al. The circuit articles disclosed in O'Bryan et al., for example the flexible circuit described with respect to FIG. 4, includes holes 46 and 46' that are electroplated with copper to form surface copper structures 47 and 47'. Such electroplated structures effect solid conducting via connections, and do not include features for significantly altering the electrical signal through the via, as is effected by the inclusion of passive components in the vias of claim 25. Furthermore, since the purpose of the electroplated structures in O'Bryan et al. is to be completely conducting, having a non-conductive wall in such via as set forth in claim 25 would destroy the signal carrying functionality of such

structures. In regard to the basic requirements of a *prima facie* case of obviousness, §2143.01 of the MPEP sets forth that "if proposed modification would render prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification."

Claim 25 as presently amended also sets forth that the first and second device layers comprise an epoxy-fiberglass composite material. The May 6, 2004 Office Action correctly notes the lack of disclosure in Takagi et al. of such a material, and suggests that the technology of Takagi et al. could be modified to include the use of an epoxy-fiberglass composite material such as disclosed in O'Bryan et al. Applicant submits that modification of the circuit substrate of Takagi et al. to be made of an epoxy-fiberglass material (e.g., FR4) as disclosed in O'Bryan et al. would render the Takagi et al. reference unsatisfactory for its intended purpose. More particularly, utilization of an epoxy-fiberglass material such as FR4 in place of the disclosed green ceramic layers would destroy the functionality of the disclosed system. The epoxy-fiberglass composite material would not survive the high processing temperatures (on the order of about 900-1000 degrees Celsius) of the system disclosed in Takagi et al. (see col. 7, lines 1-3). Also, many passive components available at the time of the present invention and integrated with the electrical device set forth in claim 25 could not survive such high processing temperatures. In regard to the basic requirements of a *prima facie* case of obviousness, §2143.01 of the Manual of Patent Examining Procedure (MPEP) sets forth that "if proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification."

Since all of the elements set forth in claim 25 as presently amended are not disclosed singularly or in combination of the Takagi et al. and O'Bryan et al. references, Applicant respectfully submits that present claim 25 is in condition for allowance and acknowledgement of the same is earnestly solicited. Also, Applicant respectfully traverses the 35 U.S.C. §103(a) rejection of claim 25 because there is no suggestion or motivation to combine the O'Bryan et al. and Takagi et al. references. More particularly, the proposed modification of Takagi et al. to incorporate the features set forth in

O'Bryan et al. would destroy the intended function of Takagi et al. Furthermore, since claims 30 and 33 variously depend from otherwise allowable claim 25 and further limit same, claims 30 and 33 should also be allowable.

REJECTION OF CLAIMS 27 and 28 (35 U.S.C. §103(a)):

Claims 27 and 28 stand rejected under 35 U.S.C. §103(a) as being obvious over Takagi et al. in view of Adae-Amoakoh et al. and O'Bryan et al. and further in view of U.S. Patent No. 5,512,710 (Schroeder).

Based on the previous remarks concerning independent claim 19, Applicant submits that present claim 19 is in complete condition for a notice of allowance. Since claims 27 and 28 variously depend from otherwise allowable claim 19 and further limit same, claims 27 and 28 should also be allowable, and acknowledgement of the same is earnestly solicited.

REJECTION OF CLAIMS 31 and 32 (35 U.S.C. §103(a)):

Claims 31 and 32 stand rejected under 35 U.S.C. §103(a) as being obvious over Takagi et al. in view of O'Bryan et al. and Schroeder.

Based on the previous remarks concerning independent claim 25, Applicant submits that present claim 25 is in complete condition for a notice of allowance. Since claims 31 and 32 variously depend from otherwise allowable claim 25 and further limit same, claims 31 and 32 should also be allowable, and acknowledgement of the same is earnestly solicited.

CONCLUSION:

Inasmuch as all outstanding issues have been addressed it is respectfully submitted that the present application, including claims 19-21 and 24-35, is in complete condition for issuance of a formal Notice of Allowance, and action to such effect is earnestly solicited. The Examiner is invited to telephone the undersigned at his convenience should only minor issues remain after consideration of this Amendment and Response in order to permit early resolution of the same.

Respectfully submitted,

DORITY & MANNING,
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